Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS**

1. **A1**
2. **B1**
3. **Y1**
4. **A2**
5. **B2**
6. **Y2**
7. **GND**
8. **Y3**
9. **A3**
10. **B3**
11. **Y4**
12. **A4**
13. **B4**
14. **Vcc**

**11 10**

**12**

**13**

**14**

**1**

**2**

**3 4**

**9**

**8**

**7**

**6**

**5**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 6E**

**APPROVED BY: DK DIE SIZE .037” X .042” DATE: 12/9/16**

**MFG: NATIONAL THICKNESS .014” P/N: DM5409**

**DG 10.1.2**

#### Rev B, 7/19/02